

REMARKS/ARGUMENTS

1. Objection to the specification:

On page 1, before "BACKGROUND OF THE INVENTION",
5 insert:

CROSS REFERENCE TO RELATED DOCUMENT

This application claims priority to Taiwanese Patent Application No.
10 092125671, filed on September 17, 2003.

Response:

The specification has been amended to add the foreign priority
information listed above. Acceptance of the amended specification is
15 respectfully requested.

2. Rejection of claims 1-16 under 35 U.S.C. 101:

Claims 1-16 are rejected under 35 U.S.C. 101 because the claimed
invention is directed to non-statutory subject matter. They fail to have
20 any of the statutory categories of: a "machine", "manufacture", and
composition of matter", which all define things or products, and a
"process", which defines actions.

Claims 1-16 are also rejected under 35 U.S.C. 101 because the
25 claimed invention is not supported by either a specific asserted utility
or a well established utility.

Response:

Independent claim 1 has been amended to overcome this rejection. Claim 1 is now directed to "A method for fabricating a routing layout design". The present invention teaches a way to fabricate metal traces on metal layers using photomasks, and to connect the metal traces using a via layer formed between the two metal layers. Claim 1 now recites a claimed method of fabricating a semiconductor device with the claimed steps, and the fabrication method defines actions that are used to build a manufactured item.

Regarding the utility of the claimed invention, paragraphs [0036]-[0037] of the specification explain the utility of the invention along with the advantages that can be realized. For example, two metal layers each contain many different horizontal and vertical metal traces that can be connected to each other through vias created using a via layer formed between the two metal layers. By changing the connections of various metal traces with the vias, the same semiconductor structure can be given a variety of different functions. In this way, the same photomasks can be used to fabricate the metal layers and the via layer of many different types of semiconductor devices, and only the via connections need to be changed to alter the functionality of the semiconductor devices. Therefore, the present invention provides great utility in reducing the number of different photomasks that are needed for fabricating different kinds of semiconductor devices. In view of the above reasons, reconsideration of claims 1-16 is respectfully requested.

3. Rejection of claims 1-16 under 35 U.S.C. 112, first paragraph:

Claims 1-16 are rejected under 35 U.S.C. 112, first paragraph since the claimed invention is not supported by either a specific asserted utility or a well established utility for the reasons set forth above, one skilled in the art would not know how to use the claimed invention.

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Response:

The utility of the claimed invention is explained with respect to the 35 U.S.C. 101 rejections above. The applicant submits that one skilled in the art would appreciate the utility of the claimed invention from reading the specification of the instant application, such as paragraphs [0036]-[0037]. As such, reconsideration of claims 1-16 is respectfully requested.

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4. Introduction to the new claims

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Claim 17 is fully supported by the application. Steps (a)-(d) are mentioned in, for example, paragraph [0024]-[0032] and Figs. 4-6. Following the example, paragraph [0024] pre-defines metal traces on a metal layer M3 and a metal layer M4 (step (a) of claim 17). Fig. 6 and paragraphs [0026]-[0027] suggest step (b) of claim 17. Paragraph [0028] and Fig. 6 lead to step (c) and (d) of claim 17. As described in paragraph [0030] and Figs. 4-5, a routing A₁-A₂ required in Place and Routing (P and R) step of Fig. 2 can be achieved by positioning vias 34a-34j (Figs. 4-5) to connect the pre-defined metal traces 24a-24c, 26b, 26k, 28a, 28b, 28c, 30a, 30k and 30l. Similarly, paragraphs [0030]-[0031] and Figs. 4-5 also describe how routings B₁-B₂ and C₁-C₂ are morphed to match the metal traces pre-defined in Figs. 4-5, and then appropriate vias can be located to achieve P and R step result shown in Fig. 2.

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Claim 18 is supported by, for example, paragraph [0030] and Figs. 4-5, where

union of the partially overlapped pre-defined metal traces 24a-24c, 26b, 26k, 28a, 28b, 28c, 30a, 30k and 30l are selected to match routing A_1 - A_2 required in P and R step of Fig. 2.

5 Claim 19 is supported in, for example, Figs. 4-5, where a second trace 26k (Fig. 4, near top of right side) overlaps a first trace 28a (Fig. 5, near top of left side) in a middle portion between two end portions of the second trace 26k, and each of the two end portions and the middle portion of the second trace 26k has a pre-defined space for positioning at least one via; e.g., a space for positioning via 34j in the end
10 portion of the second trace 26k and a space for positioning via 34i in the middle portion of the second trace 26k.

 Claim 20 is supported by, for example, paragraph [0036] (starting from line 8, "When the routing design is changed...") and paragraph [0037] (starting from line 7,
15 "Accordingly, the photomasks for defining the metal trace arrangements...can be reused when...produces two different kinds of ICs...")

 These new claims are fully supported by the original application and no new matter is introduced. Also, these new claims emphasize one of the major advantages
20 (and utilities) of the application: using a reusable metal layer layout design to meet different routing requirements by changing via layout only. In this way, the cost, time, and resources for designing and fabricating ICs can be greatly reduced.

 Applicant respectfully requests that a timely Notice of Allowance
25 be issued in this case.

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Reply to Office action of August 15, 2006

Sincerely yours,

Winston Hsu

Date: 11.14.2006

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- 10 Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)